



Docket No.: 08211/0200655-US0 (P05800)  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Hidehiko Suzuki

Allowed: January 25, 2006

Application No.: 10/823,291

Confirmation No.: 4557

Filed: April 13, 2004

Art Unit: 2816

For: APPARATUS AND METHOD FOR  
REDUCING PROPAGATION DELAY

Examiner: T. Hiltunen

**COMMENTS ON STATEMENT OF REASONS  
FOR ALLOWANCE UNDER 37 CFR §1.104(E)**

MS Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Applicant has received the Examiner's Statement of Reasons for Allowance with the January 25, 2006 Notices of Allowance and Allowability regarding the above-identified application. Entry of the Statement into the record should not be construed as any agreement with or acquiescence in the reasoning stated by the Examiner. Each of the claims stands on its own merits and is patentable because of the combination it recites and not because of the presence or absence of any one particular element.

The Examiner's Statement was not prepared by Applicant and only contains the Examiner's possible positions in one or more reasons for allowability. Thus, any interpretation with

The Examiner's Statements of Reasons for Allowance states, regarding a proposed combination of Kong and and Sanyo, "However, the offset circuit does not output a value approximately equal to  $V_{dd} + I_1 * R_1$ , where  $V_{DD} + I_1 * R_1$  is equal to the difference between a high and low voltage. Therefore claim 21 is deemed allowable." This appears to contain a misstatement of what claim 21 requires. Claim 21 does not recite outputting a value approximately equal to  $V_{dd} + I_1 * R_1$ . Rather, Claim 21 recites that "the logic circuit performs as if the difference between the high power supply and the low power supply was approximately  $V_{DD} + I_1 * R_1$ ".

Respectfully submitted,

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